UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,134	04/04/2001	David K. Vavro	INTL-0546-US (P11105)	2324

		EXAMINER
7590	02/07/2005	MEONSKE, TONIA L

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ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 02/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/826,134	VAVRO, DAVID K.
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2.   Claims 1-30 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by

Hennessy, et al., *Computer Architecture a Quantitative Approach*, Morgan Kaufman Publishers

Inc., Second Edition, pages 246-251 (hereinafter "Hennessy").

3.   The rejections are respectfully maintained and incorporated by reference as set forth in

the last office action, mailed on September 16, 2004.

Response to Arguments

4.   Applicant's arguments filed November 15, 2004 have been fully considered but they are

not persuasive.

5.   On page 3, Applicant argues with respect to claim 1 and similarly with respect to claim

18 in essence:

> *"All of the claims were rejected over a couple of pages out of a computer architecture book. The material cited is so vague and incomplete that there is no basis whatsoever to conclude that the so-called functional units constitute separate processors. Therefore, a prima facie rejection is not made out, since there is no showing that a register is accessible by a plurality of processors.*
> *There is no reason to believe that the functional units are separate processors. Moreover, there is no indicating whether data in said register is available for a given processor. To show this element, five pages are cited in Figure 4.4. But Figure 4.4 shows nothing of the sort and the five pages have nothing informative."*

However, a processor is merely something that operates on data. A functional unit operates on, or processes, data. Therefore a functional unit is a processor. So Hennessey has in fact taught a plurality of processors, i.e. Integer, Mult1, Mult2, Add, Divide (See Figure 4.4). Furthermore, each register i.e. F0-F30 in Figure 4.4, is inherently accessible by all of the functional units. It is clear from Figure 4.4 that register F2 is accessible to at least the Integer, Mult1, and Add functional units. Therefore, Hennessy has in fact taught that a register, F2, is accessible by a plurality of processors, Integer, Mult1, and Add functional units. Therefore this argument is moot.

6.   On page 3, Applicant argues with respect to claim 1 and similarly with respect to claim 18 in essence:

> "There is no indicating whether data in said register is available for a given processor.
> To show this element, five pages are cited in Figure 4.4. But Figure 4.4 shows nothing
> of the sort and the five pages have nothing informative."

However, Hennessy has taught whether data in a register is available for a given processor. Referring to Figure 4.4, the second LD instruction is to write a result to register F2. As soon as the result is written into F2, the result is available to other instructions and functional units using F2 as a source operand. In this instance the result has not yet been written into F2, and as such the result is not yet available for the Mult1 functional unit. Therefore, Hennessy has in fact taught indicating whether data in said register, F2, is available for a given processor, Mult1 (Figure 4.4 indicates that data in F2 is not yet available for processor Mult1.). Therefore this argument is moot.

7.   On page 3, Applicant argues in essence:

> "There is no structure shown and, therefore, it cannot be determined that a register is
> coupled to said processing elements."

However, in Hennessy the functional units are the processing elements, i.e. Integer, Mult1, Mult2, Add, and Divide. In Figure 4.4, F2 is: 1) a destination register for a result from the Integer functional unit, 2) a source register for the Mult1 functional unit, and 3) a source register for the Add functional unit. In order for the functional units to receive source data from F2 and/or output destination data to F2, F2 must inherently be coupled, either directly or indirectly, to the functional units. Therefore this argument is moot.

8.   On page 3, Applicant argues in essence:

"Moreover, there is no indication in the material cited that the register includes a plurality of general purpose registers."

Applicant is directed to Figure 4.4 of Hennessy. F0-F30 are the claimed general purpose registers. Therefore this argument is moot.

Conclusion

9.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

10.   A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.
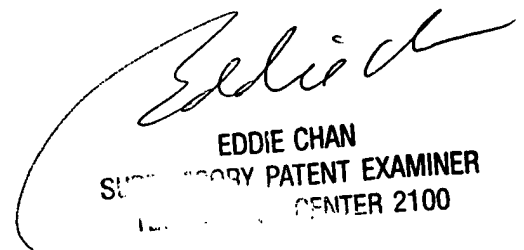
11.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tonia L Meonske whose telephone number is (571) 272-4170.

The examiner can normally be reached on Monday-Friday, 8-4:30.

12.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie P Chan can be reached on (571) 272-4162. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

13.   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

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